FORM PTO-1390 (REV 9-2001) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY 'S DOCKET NUMBER: 085907-000000US

U S APPLICATION NO (If known, see 37 CFR 1 5): unassigned 10/070013

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/CA00/00995	01 September 2000 (01.09.2000)	01 September 1999 (01.09.1999)

TITLE OF INVENTION
IMPROVED METHOD AND APPARATUS FOR UP-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS

APPLICANT(S) FOR DO/EO/US
MANKU, Tajinder, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST submission of items concerning a filing under 35 U.S.C. 371.**
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 36 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U S.C. 371(f). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 37(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.2 and 35 U.S.C. 1.821 – 1.825.
18. ☐ A second copy of the published international application under 36 U.S.C.
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information:

a. Express Mail Label No. EL585155653US mailed on February 28, 2002
b. Return Postcard
c. International Publication No. WO 01/17121 A1
d. Written Opinion
e. Response to Written Opinion

I/S/ Application no. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
unassigned 10/070013	PCT/CA00/00995	085907-000000US

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(A) (1) – (5)):	CALCULATIONS PTO USE ONLY	
Neither international preliminary examination fee (37 CFR 1.492) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search report prepared by the EPO of JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1 482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$890.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	**$0**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	31 - 20 =	11	x **$18.00**	$198.00	
Independent claims	2-3 =	0	x **$84.00**	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **280.00**	$0	
			TOTAL OF ABOVE CALCULATIONS =	$198.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$0	
			SUBTOTAL =	$1088.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFT 1.492(f)				$0	
			TOTAL NATIONAL FEE =	$1088 00	
Fee for recording the enclosed assignment (37 CFR 1.2(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3 31). **$40.00** per property			+	$0	
			TOTAL FEES ENCLOSED =	$1088.00	
			Amount to be refunded:	$0	
			charged:	$1088 00	

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 20-1430 in the amount of $1088 00 to cover the above fees.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-1430. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Townsend and Townsend and Crew LLP
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Kenneth R. Allen
SIGNATURE

February 28, 2002
DATE

Kenneth R. Allen
NAME

27,301
REGISTRATION NUMBER

PATENT

Attorney Docket No. 085907-000000US
Client Reference No. 08887953US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MANKU, Tajinder

Application No.: Not yet assigned

Filed: Herewith

For: IMPROVED METHOD AND APPARATUS FOR UP-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the examination of the above-referenced application, please enter the following amendments.

IN THE CLAIMS:

Applicants respectfully submit previous amendments to the claims that were made pursuant Article 34 in response to the Written Opinion during the International Phase and at this time, Applicants have re-formatted the claims in accordance with preferred U.S. patent practice to delete claims 30, 33 and 34 and to eliminate the multiple dependency in claim 32.

Respectfully submitted,

Kenneth R. Allen

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WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal *x(t)* φ_1 φ_2; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1$; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2

31. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi 1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said mixing signal φ_1; to generate an output signal $x(t)\ \varphi_1$; and

mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

32. An integrated circuit comprising the radio frequency (RF) up-convertor of claim 1.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said ~~time-varying~~mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said ~~time-varying~~mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal *x(t)* φ_1 φ_2.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal *x(t)* φ_1 φ_2; and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where said ~~time-varying~~mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, ~~further comprising~~where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying signals are irregular~~synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-converter of claim 3, further comprising:

a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~ mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, ~~further comprising: a filter for removing unwanted signal components~~: where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

~~30. The radio frequency (RF) up-converter of claim 1, further comprising: a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.~~

31. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating ~~time-varying~~ mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi 1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said ~~time-varying~~ mixing signal φ_1; to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)$ φ_1 with said ~~time-varying~~ mixing signal φ_2 to generate an output signal $x(t)$ φ_1 φ_2.

32. An integrated circuit comprising the radio frequency (RF) up-convertor of ~~any one of claims 1-30~~ claim 1.

~~33. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1-30.~~

~~34. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1-30.~~

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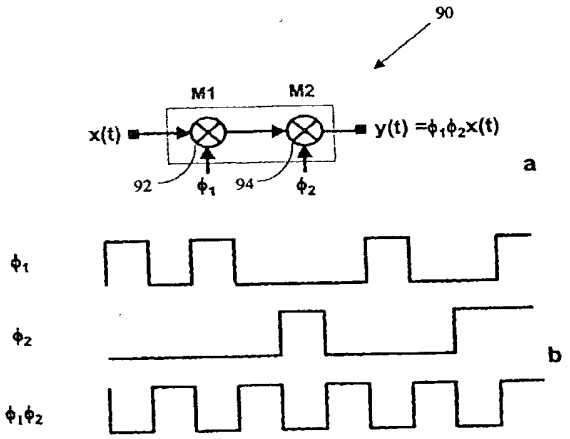
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: IMPROVED METHOD AND APPARATUS FOR UP-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS



(57) Abstract: This patent describes a method and system which overcomes the LO-leakage problem of direct conversion and similar RF transmitters. To solve this problem a virtual LO™ signal is generated within the baseband which is tuned to the incoming RF signal. The virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the wanted output RF frequency. Any errors in generating the virtual LO signal are minimized using a closed loop correction scheme.

WO 01/17121 A1

10/pRTS

Improved Method and Apparatus for Up-Conversion of Radio Frequency (RF) Signals

The present invention relates generally to communications, and more specifically, to a fully-integrable method and apparatus for up-conversion of radio frequency (RF) and baseband signals with reduced local oscillator (LO) leakage.

Background of the Invention

Many communication systems modulate electromagnetic signals from baseband to higher frequencies for transmission, and subsequently demodulate those high frequencies back to their original frequency band when they reach the receiver. The original (or baseband) signal, may be, for example: data, voice or video. These baseband signals may be produced by transducers such as microphones or video cameras, be computer generated, or transferred from an electronic storage device. In general, the high transmission frequencies provide longer range and higher capacity channels than baseband signals, and because high frequency RF signals can propagate through the air, they can be used for wireless channels as well as hard wired or fibre channels.

All of these signals are generally referred to as radio frequency (RF) signals, which are electromagnetic signals, that is, waveforms with electrical and magnetic properties within the electromagnetic spectrum normally associated with radio wave propagation. The electromagnetic spectrum was traditionally divided into 26 alphabetically designated bands, however, the ITU formally recognizes 12 bands, from 30 Hz to 3000 GHz. New bands, from 3 THz to 3000 THz, are under active consideration for recognition.

Wired communication systems which employ such modulation and demodulation techniques include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet. These networks generally communication data signals over electrical or optical fibre chanels. Wireless communication systems which may employ modulation and demodulation include those for public broadcasting such as AM and FM radio, and UHF and VHF television. Private communication systems may include cellular telephone networks, personal paging devices, HF radio systems used by taxi services, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications. Other wired and

wireless systems which use RF modulation and demodulation would be known to those skilled in the art.

One of the current problems in the art, is to develop physically small and inexpensive modulation techniques and devices that have good performance characteristics. For cellular telephones, for example, it is desirable to have a transmitter which can be fully integrated onto an integrated circuit.

Several attempts have been made at completely integrating communication transmitter designs, but have met with limited degrees of success. Existing solutions and their associated problems and limitations are summarized below:

1. Direct Conversion Transmitter

Direct conversion architectures **10** modulate baseband signals to RF levels in a single step by mixing a baseband signal with a local oscillator signal at the carrier frequency. Referring to the block diagram of **Figure 1**, the in-phase (I) and quadrature (Q) components of the baseband signal are up-converted to RF via mixers MI **12** and MQ **14**, respectively. The RF mixing signals are generated using a local oscillator **16** tuned to the RF, and a 90 degree phase shifter **18** which ensures that the I and Q signals are up-converted into their quadrature components. The two up-converted RF signals are added together via the summing element S **20**, and filtered via a band pass filter (BPF) **22** having a pass band response around the RF signal to remove unwanted components. Finally, a power amplifier (PA) **26** amplifies the signal to the necessary transmission level.

Generally, a mixer is a circuit or device that accepts as its input two different frequencies and presents at its output:

(a) a signal equal in frequency to the sum of the frequencies of the input signals;

(b) a signal equal in frequency to the difference between the frequencies of the input signals; and

(c) the original input frequencies.

The typical embodiment of a mixer is a digital switch, which may generate significantly more tones than those shown above.

Hence, the disadvantages of this topology are:

- the LO signal leaks into the RF signal. since the RF output signal is at the same frequency as the LO signal; and
- the output RF signal leaks back into the LO generation elements, causing it to detune. This mechanism is commonly referred to "LO pulling".

However, this topology can easily be integrated and requires fewer components than other modulation topologies known in the art.

2. Directly Modulated Transmitter

Figure 2 presents a block diagram of a directly modulated transmitter **30** in which the baseband signal modulates a voltage control oscillator (VCO) **32**, designed to oscillate within the vicinity of the RF frequency. The output of the VCO **32** is then filtered by a bandpass filter (BPF) **34** which has a pass band around the RF frequency to remove unwanted components. A power amplifier **36** then amplifies the filtered signal to the amplitude required.

The disadvantages of this topology are:

- the LO signal leaking into the RF signal; and
- the output RF signal leaking back into the LO generation element, causing it to detune. Again, this mechanism is commonly referred to "LO pulling".

This topology can easily be integrated and requires a small number of components. To maintain stability, the VCO **32** is locked via a phase lock loop in most applications. In some applications, the input to the VCO **32** could be an up-converted version of the baseband signal.

3. Dual Conversion Transmitter

A dual conversion topology solves two of the problems associated with the direct conversion and the direct modulation topologies, specifically, the LO signal leaking into the RF signal and "LO pulling". In this topology the baseband signal is translated to the RF band via two frequency translations, which are associated with two local oscillators (LOs), neither of which is tuned to the RF signal. Because neither of these LOs are tuned to the desired RF output frequency, the LO leakage problem and "LO pulling" problem are generally eliminated.

The dual conversion topology is presented as a block diagram in **Figure 3**. Like the direct conversion transmitter described with respect to **Figure 1** hereinabove, the in-phase (I) and quadrature (Q) components of the base-band signal are first up-converted to RF via the mixers MI **42** and MQ **44**, respectively. However, in this case, the RF mixing signal generated using local oscillator **46** is not tuned to the desired output frequency, but is tuned to an intermediate frequency (IF). The 90 degree phase shifter **48** then ensures that the I and Q signals are up-converted into their quadrature IF components. The two-upconverted IF signals are then added together via the summing element S **50**, and filtered via a band pass filter (BPF) **52** having a pass band response around the IF signal.

The IF signal is then up-converted to the desired RF output frequency via mixer M **54** and a second local oscillator (LO2) **55**, which need not be at the RF output frequency. The signal is then filtered via a second band pass filter (BPF) **56** having a pass band around the RF signal, and is amplified to the desired level using power amplifier (PA) **26**.

Though this technique addresses the problems with the direct conversion and the direct modulation topologies, it has disadvantages of its own:

- it requires two LO signals;
- it requires two filters;
- it requires a significant amount of frequency planning; and
- it is difficult to integrate all the components into an integrated circuit.

4. Offset Conversion Transmitter

An offset conversion topology **60** such as that presented in **Figure 4**, also solves the two main problems associated with direct conversion and direct modulation, that is, the LO signal leaking into the RF signal and "LO pulling". Like the dual conversion transmitter, this is done by translating the baseband signal to the RF band using two local oscillators, neither of which are tuned to the RF output frequency. As noted above, the LO leakage problem and "LO pulling" problem are avoided, because neither of these LOs are tuned to the RF output frequency.

Referring to the block diagram of **Figure 4**, the baseband signal is up-converted to the RF frequency via mixers MI **62** and MQ **64** which are modulated by a combined signal from two separate oscillators LO1 **66** and LO2 **68**. The frequency used to up-convert the base band signal is equal to f1 + f2 where f1 is the fundamental frequency component of the local oscillator LO1 **66** signal and f2 is the fundamental component of the local oscillator LO2 **68** signal. Mixing the signals from oscillators LO1 **66** and LO2 **68** via the mixer M **70** generates the frequency f1 + f2, which corresponds to the RF output frequency. A band pass filter (BPF) **72** is then used to attenuate all frequency components except f1 + f2. The 90 degree phase shifter **74** ensures the I and Q signals are up-converted into their quadrature components.

The two-upconverted signals are then added together via the summing element S **76**, and filtered via a band pass filter (BPF) **78** having a pass band around the RF signal. Finally, a power amplifier **80** amplifies the signal to the desired level.

The disadvantages of this topology are:

- it requires two LO signals;
- it requires two filters; and
- it requires a significant amount of frequency planning.

There is therefore a need for a method and apparatus of modulating RF signals which allows the desired integrability along with good performance.

Summary of the Invention

It is therefore an object of the invention to provide a novel method and system of modulation which obviates or mitigates at least one of the disadvantages of the prior art.

One aspect of the invention is broadly defined as a radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal $x(t)$, comprising: a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of the local oscillator signal being emulated; a first mixer coupled to the synthesizer for mixing the input signal $x(t)$ with the time-varying signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and a second mixer coupled to the synthesizer and to the output of the first mixer for mixing the signal $x(t)\ \varphi_1$ with the time-varying signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

Brief Description of the Drawings

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings in which:

Figure 1 presents a block diagram of a direct conversion transmitter as known in the art;

Figure 2 presents a block diagram of a directly modulated transmitter as known in the art;

Figure 3 presents a block diagram of a dual conversion transmitter as known in the art;

Figure 4 presents a block diagram of offset conversion transmitter as known in the art;

Figure 5 (a) presents a block diagram of a broad implementation of the invention;

Figure 5 (b) presents exemplary mixer input signals functions φ_1 and φ_2 plotted in amplitude against time;

Figure 6 presents a block diagram of quadrature modulation in an embodiment of the invention;

Figure 7 presents a block diagram of an embodiment of the invention employing error correction by measuring the amount of power at baseband;

Figure 8 presents a block diagram of a transmitter in a preferred embodiment of the invention;

Figure 9 presents a block diagram of an embodiment of the invention employing a filter placed between mixers M1 and M2; and

Figure 10 presents a block diagram of an embodiment of the invention employing N mixers and N mixing signals.

Detailed Description of Preferred Embodiments of the Invention

A device which addresses the objects outlined above, is presented as a block diagram in **Figure 5(a)**. This figure presents a modulator topography **90** in which an input signal *x(t)* is mixed with signals which are irregular in the time domain (TD), which effect the desired modulation. A virtual local oscillator (VLO) is generated by multiplying two functions (labelled φ_1 and φ_2) within the signal path of the input signal *x(t)* using two mixers M1 **92** and M2 **94**. The mixers described within this invention would have the typical properties of mixers within the art, that is, they would have an associated noise figure, linearity response, and conversion gain. The selection and design of these mixers would follow the standards known in the art, and could be, for example, double balanced mixers. Though this figure implies various elements are implemented in analogue form they can be implemented in digital form.

The two time-varying functions φ_1 and φ_2 that comprise the virtual local oscillator (VLO) signal have the property that their product emulates a local oscillator (LO) signal that has significant power at the carrier frequency, but neither of the two signals has a significant level of power at the frequency of the local oscillator being emulated. As a result, the desired modulation is affected, but there is no LO signal to leak in the RF path. **Figure 5b** depicts possible functions for φ_1 and φ_2.

To minimize the leakage of LO power into the RF output signal, as in the case of direct conversion and directly modulated topologies, the preferred criteria for selecting the functions φ_1 and φ_2 are:

(i) that φ_1 and φ_2 do not have any significant amount of power at the output frequency. That is, the amount of power generated at the output frequency should not effect the overall system performance of the transmitter in a significant manner;

(ii) the signals required to generate φ_1 and φ_2 should not have a significant amount of power at the output frequency; and

(iii) if x(t) is a baseband signal, $\varphi_1 * \varphi_1 * \varphi_2$ and $\varphi_2 * \varphi_2$ should not have a significant amount of power within the bandwidth of the up-converted RF (output) signal.

Conditions (i) and (ii) ensure an insignificant amount of power is generated within the system at the frequencies which would cause an equivalent LO leakage problem found in conventional direct conversion and directly modulated topologies. Condition (iii) ensures that if φ_1 leaks into the input port, it does not produce a signal within the RF signal at the output. Condition (iii) also ensures that if φ_2 leaks into node between the two mixers, it does not produce a signal within the RF signal at the output.

Various functions can satisfy the conditions provided above, several of which are described hereinafter, however it would be clear to one skilled in the art that other similar pairs of signals may also be generated. These signals can in general be random, pseudo-random, periodic functions of time, or digital waveforms. While these signals may be described as "aperiodic", groups of cycles may be repeated successively. For example, the φ_1 and φ_2 signals presented in **Figure 5(b)** which generate the five-cycle $\varphi_1 * \varphi_2$ signal, may be input to mixers M1 **92** and M2 **94** repeatedly.

As well, rather than employing two mixing signals shown above, sets of three or more signals may be used (additional description of this is given hereinafter with respect to **Figure 10**).

It would also be clear to one skilled in the art that virtual LO signals may be generated which provide the benefits of the invention to greater or lesser degrees. While it is possible in certain circumstances to have almost no LO leakage, it may be acceptable in other circumstances to incorporate apply virtual LO signals which still allow a degree of LO leakage.

The topology of the invention is similar to that of direct up-conversion, but provides a fundamental advantage: minimal leakage of a local oscillator (LO) signal into the RF band. The topology also provides technical advantages over other known topologies such as directly modulated, dual conversion and offset conversion transmitters:

- removes the necessity of having a second LO and various (often external) filters; and
- has a higher level of integration as the components it does require are easily placed on an integrated circuit.

While the basic implementation of the invention may produce errors in generating the virtual local oscillator (VLO), solutions to this problem are available and are described hereinafter.

The invention provides the basis for a fully integrated communications transmitter. Increasing levels of integration have been the driving impetus towards lower cost, higher volume, higher reliability and lower power consumer electronics since the inception of the integrated circuit. This invention will enable communications transmitters to follow the same integration route that other consumer electronic products have benefited from.

Specifically, advantages from the perspective of the manufacturers when incorporating the invention into a product include:

1. significant cost savings due to the decreased parts count of an integral device. Decreasing the parts count reduces the cost of inventory control, reduces the costs associated with warehousing components, and reduces the amount of manpower to deal with higher part counts;
2. significant cost savings due to the decreased manufacturing complexity. Reducing the complexity reduces time to market, cost of equipment to manufacture the product, cost of testing and correcting defects, and reduces time delays due to errors and problems on the assembly line;
3. reduces design costs due to the simplified architecture. The simplified architecture will shorten the first-pass design time and total design cycle time as a simplified design will reduce the number of design iterations required;
4. significant space savings and increased manufacturability due to the high integrability and resulting reduction in product form factor (physical size). This implies huge savings throughout the manufacturing process as smaller device footprints enable manufacturing of products with less material such as

printed circuit substrate, smaller product casing and smaller final product packaging;

5. simplification and integrability of the invention will yield products with higher reliability, greater yield, less complexity, higher life span and greater robustness;

6. due to the aforementioned cost savings, the invention will enable the creation of products that would otherwise be economically unfeasible;

Hence, the invention provides the manufacturer with a significant competitive advantage.

From the perspective of the consumer, the marketable advantages of the invention include:

1. lower cost products, due to the lower cost of manufacturing;
2. higher reliability as higher integration levels and lower parts counts imply products will be less prone to damage from shock, vibration and mechanical stress;
3. higher integration levels and lower parts counts imply longer product life span;
4. lower power requirements and therefore lower operating costs;
5. higher integration levels and lower parts counts imply lighter weight products;
6. higher integration levels and lower parts counts imply physically smaller products; and
7. the creation of economical new products.

The present invention relates to the translation of a baseband signal directly to an RF signal and is particular concerned with solving the LO-leakage problem associated with the present art. The invention allows one to fully integrate a RF transmitter on a single chip without using external filters, while furthermore, the RF transmitter can be used as a multi-standard transmitter. Descriptions of exemplary embodiments follow.

In many modulation schemes, it is necessary to modulate both I and Q components of the input signal, which requires a modulator 100 as presented in the block diagram of **Figure 6**. In this case, four modulation functions would have to be generated: $\varphi_{1I} * \varphi_{2I}$ which is 90 degrees out of phase with $\varphi_{1Q} * \varphi_{2Q}$. The pairing of signals φ_{1I} and φ_{2I} must meet the function selection criteria listed above, as must the signal pairing of φ_{1Q} and φ_{2Q}. The mixers 102, 104, 106, 108 are standard mixers as known in the art.

As shown in **Figure 6**, mixer **102** receives the input signal *x(t)* and modulates it with φ_{1I}; subsequent to this, mixer **104** modulates signal *x(t)* φ_{1I} with φ_{2I} to yield the in-phase component of the input signal at baseband, that is, *x(t)* $\varphi_{1I}\varphi_{2I}$. A complementary process occurs on the quadrature side of the modulator, where mixer **106** receives the input signal *x(t)* and modulates it with φ_{1Q}; after which mixer **108** modulates signal *x(t)* φ_{1Q} with φ_{2Q} to yield the quadrature phase component of the input signal at baseband, that is, *x(t)* $\varphi_{1Q}\varphi_{2Q}$. The in-phase and quadrature components of the up-converted signal are then combined using summer **110** to yield the output signal: *x(t)* $\varphi_{1I}\varphi_{2I}$ + *x(t)* $\varphi_{1Q}\varphi_{2Q}$.

In the analysis above timing errors that would arise when constructing the *VLO* have been neglected (timing errors can be in the form of a delay or a mismatch in rise/fall times). In the analysis which follows, only delays are considered, but the same analysis can be applied to rise/fall times. The actual *VLO* that is generated can be written as:

$$VLO_a = VLO_i + \varepsilon_{VLO}(t) \qquad (1)$$

where VLO_a is the actual *VLO* generated, VLO_i is the ideal *VLO* without any timing error, and $\varepsilon_{VLO}(t)$ absorbs the error due to timing errors. Therefore, the output signal of the virtual LO topology, denoted as y(t), becomes:

$$y(t) = x(t) \times [VLO_i + \varepsilon_{VLO}(t)] \qquad (2)$$

The term *x(t) VLOi* is the wanted term and *x(t)* $\varepsilon_{VLO}(t)$ is a term that could produce aliasing power into the wanted RF signal at the output of the structure. The term $\varepsilon_{VLO}(t)$ can also be thought of a term that raises the noise floor of the *VLO*. This is not that serious a problem because the signal *x(t)* is at baseband and has a well defined bandwidth. By selecting φ_1 and φ_2 carefully and by placing an appropriate filter at the input of the structure, the amount of aliasing power can be reduced significantly, though it can never be completely eliminated due to timing errors.

There are several ways one could further reduce the amount of aliasing power, for example, by using a closed loop configuration as described below. The term *x(t)* $\varepsilon_{VLO}(t)$ contains two terms at the RF output:

(i) aliasing power P_a, and

(ii) power of the wanted signal, but at a reduced power level which is on the order of delay error P_{wt}

Therefore, the total power at the RF output (denoted by P_M) can be decomposed into three components:

(i) the power of the wanted RF signal, P_w,

(ii) the power of the aliasing terms, P_a, and

(iii) the power of the wanted RF signal arising from the term, $P_{wε}$ (this power can either be positive or negative). Therefore,

$$P_M = P_w + P_{wε}(\tau) + P_a(\tau) \qquad (3)$$

Note that $P_{wε}$ and P_a are a function of the delay τ. Since $|P_w|>>|P_{wε}|$, (3) becomes,

$$P_M = P_w + P_a(\tau) \qquad (4)$$

If the power, P_M is measured and τ is adjusted in time, one can reduce the term Pa to zero (or close to zero). Mathematically this can be done if the slope of P_M with the delay τ is set to zero; that is:

$$\frac{dP_M}{d\tau} = \frac{dP_a(\tau)}{d\tau} = 0 \qquad (5)$$

A transmitter **120** for implementing this procedure is illustrated in **Figure 7** (a more detailed description is provided in the paragraph below). The power measurement scheme and the element blocks required to detect when $\frac{dP_M}{d\tau} = 0$, can be implemented within a digital signal processing unit (DSP). Also illustrated in **Figure 7** is a visual representation of the power measured versus delay, which identifies an optimum point at which $\frac{dP_M}{d\tau} = 0$.

In the block diagram of **Figure 7** the baseband signal is first multiplied by the signals φ_1 and φ_2 via mixers M1 **122** and M2 **124**, respectively. The signal is next filtered via a band pass filter (BPF) **126**, which is used to reduce the amount of out-of-band power, which may cause the subsequent elements to compress in gain or distort the wanted signal. The design of this BPF **126** depends on the bandwidth of the wanted signal, the system specifications and system design trade offs. In the interest of simplicity, separate in-phase and quadrature channels have not been identified, though the invention is preferably implement as such.

The output of the BPF **126** is the desired up-converted RF signal. This output signal is measured with power measurement unit **128**. The power is minimized with respect to the delay added onto the signal φ_2 by use of

the $\frac{dP_M}{d(delay)} = 0$ detector **130**, and the delay controller **132** which manipulates the φ_2 signal source **134**. As shown in the timing diagram of **Figure 7**, this process allows signal φ_2 to be delayed in time.

In general, the power can be minimized with respect to the rise time of φ_2 or a combination of delay and rise time. Furthermore, the power can be minimized with respect to the delay, rise time, or both delay and rise time of the signal φ_1, or both φ_1 and φ_2. It would be clear to one skilled in the art that current or voltage may be measured rather than power in certain applications. As well, the phase delay of either or both of φ_1 and φ_2 may be modified to minimized the error.

It is preferred that this power detection **130** be done within a digital signal processing unit (DSP) **136** after the baseband signal is digitized via an analog to digital converter, but it may be done with separate components, or analogue components.

A problem that may prove to be more serious than aliasing power at the output, is a direct current offset accompanying the signal baseband signal *x(t)*. Letting *DC* represent the value of this unknown direct current offset, the input can be written as *x(t) + DC*. Therefore, the output of the structure would be of the form:

$$y(t) = x(t) \times [VLO_i] + DC \times VLO_i \qquad (6)$$

assuming there is no error associated with the generation of the *VLO* signal. In this presentation, the term $DC \times VLO_i$ represents unwanted power near the wanted signal $x(t) \times VLO_i$.

One method that can be used to remove this unwanted power, $DC \times VLO_i$, is to remove the DC offset using a calibration routing as presented in **Figure 8**. Briefly, the calibration routing of this transmitter **120** first sets the baseband signal to zero, then measures the output power, minimizing it against a parameter that adds an additional DC offset to the input of the structure via a summing device. The power measured can be made at any point after the two mixers, that is, it could be made at the output of a power amplifier driving the antenna.

Specifically, **Figure 8** presents a block diagram of a transmitter which produces a filtered and amplified baseband signal in generally the same manner as that of **Figure 7**. Hence, components **122**, **124** and **126** of **Figure 7** correspond with

components **142**, **144** and **146** of **Figure 8** respectively, though their input signals are slightly different.

It is preferred to generate the inputs to the two mixers **142** and **144** by me of signal generation blocks **148** and **150**; signal generation block **148** generating φ_1 signal and signal generation block **150** generating the φ_2 signal. Implementing the invention with separate I and Q channels would require four mixers, two per channel, and four φ signals; specifically, $\varphi_1 I$ and $\varphi_1 Q$; and $\varphi_2 I$ and $\varphi_2 Q$, as shown **Figure 6**.

The input to these generation blocks **148** and **150** is an oscillator which do not have a significant amount of signal power at the frequency of the desired outp RF signal. The construction of the necessary logic for these components would b clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 5**. Such signals may be generated using basic logic gates, fi programmable gate arrays (FPGA), read only memories (ROMs), micro-controller or other devices known in the art. Further description and other means of genera such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. PCT/CA00/00996.

The embodiment of **Figure 8** is distinct from that of **Figure 7** with regard t the feedback control loop. Power measurement of the RF output signal is perform by the power measurement unit **152**, but rather than optimising for $\frac{dP_M}{d(delay)} = 0$

per the embodiment presented in **Figure 7**, the control loop is optimised for $\frac{dP_M}{d(DCoffset)} = 0$ using detector **154**, which drives the DC offset generator **156**

DC offset is affected in the baseband signal by means of the summer **158** which sums the input baseband signal with the direct current offset from the DC offset generator **156**. Suitable components for the DC offset generator **156** and summe **158** are known in the art.

The physical order (that is, arrangement) of the BPF **146**, the DC offset correction summer **158**, and any additional gain control elements (none shown) ca be rearranged to some degree. Such modifications would be clear to one skilled i the art.

As in the case of **Figure 7**, separate in-phase and quadrature channels have not been identified in the interest of simplicity, though the invention of **Figure 8** is preferably implement as such. As well, though the figure implies the use of analogue components, they can be implemented in digital form.

Also as in the case of **Figure 7**, it is preferred that the detector **154**, be embodied in a digital signal processor (DSP) **160**.

It would be clear to one skilled in the art that many variations may be made to the designs presented herein, without departing from the spirit of the invention. One such variation to the basic structure in **Figure 5a** is to add a filter **170** between the two mixers **92** and **94** as shown in the block diagram of **Figure 9** to remove unwanted signals that are transferred to the output port. This filter **170** may be a low pass, high pass, or band pass filter depending on the transmitter requirements. The filter **170** does not necessarily have to be a purely passive filter, that is, it can have active components.

Another variation is that several functions φ_1, φ_2, φ_3 ... φ_n may be used to generate the virtual LO, as presented in the block diagram of **Figure 10**. Here, φ_1* φ_2*... *φ_n has a significant power level at the LO frequency, but each of the functions φ_1... φ_n contain an insignificant power level at LO.

The electrical circuits of the invention may be described by computer software code in a simulation language, or hardware development language used to fabricate integrated circuits. This computer software code may be stored in a variety of formats on various electronic memory media including computer diskettes, CD-ROM, Random Access Memory (RAM) and Read Only Memory (ROM). As well, electronic signals representing such computer software code may also be transmitted via a communication network.

Clearly, such computer software code may also be integrated with the code of other programs, implemented as a core or subroutine by external program calls, or by other techniques known in the art.

The embodiments of the invention may be implemented on various families of integrated circuit technologies using digital signal processors (DSPs), microcontrollers, microprocessors, field programmable gate arrays (FPGAs), or discrete components. Such implementations would be clear to one skilled in the art.

The invention may be applied to various communication protocols and formats including: amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), phase shift keying (PSK), cellular telephone systems including

analogue and digital systems such as code division multiple access (CDMA), time division multiple access (TDMA) and frequency division multiple access (FDMA).

The invention may be applied to such applications as wired communication systems include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet, using electrical or optical fibre cable systems. As well, wireless communication systems may include those for public broadcasting such as AM and FM radio, and UHF and VHF television; or those for private communication such as cellular telephones, personal paging devices, wireless local loops, monitoring of homes by utility companies, cordless telephones including the digital cordless European telecommunication (DECT) standard, mobile radio systems, GSM and AMPS cellular telephones, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications.

While particular embodiments of the present invention have been shown and described, it is clear that changes and modifications may be made to such embodiments without departing from the true scope and spirit of the invention.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, fc modulating an input signal *x(t)*, comprising:

a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillatc signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signa $x(t)\ \varphi_1\ \varphi_2$.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1\ \varphi_2$; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltag to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

30. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of sai local oscillator signal being emulated;

mixing said input signal $x(t)$ with said mixing signal φ_1 to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)$ φ_1 with said mixing signal φ_2 to generate an output signal $x(t)$ φ_1 φ_2.

31. An integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

32. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29

33. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1 - 29.

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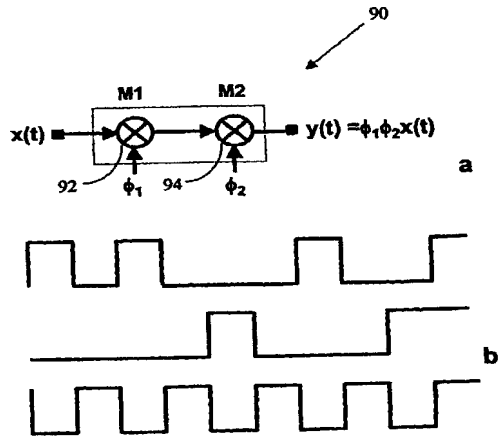
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: IMPROVED METHOD AND APPARATUS FOR UP-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS



(57) Abstract: This patent describes a method and system which overcomes the LO-leakage problem of direct conversion and similar RF transmitters. To solve this problem a virtual LO™ signal is generated within the baseband which is tuned to the incoming RF signal. The virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the wanted output RF frequency. Any errors in generating the virtual LO signal are minimized using a closed loop correction scheme.

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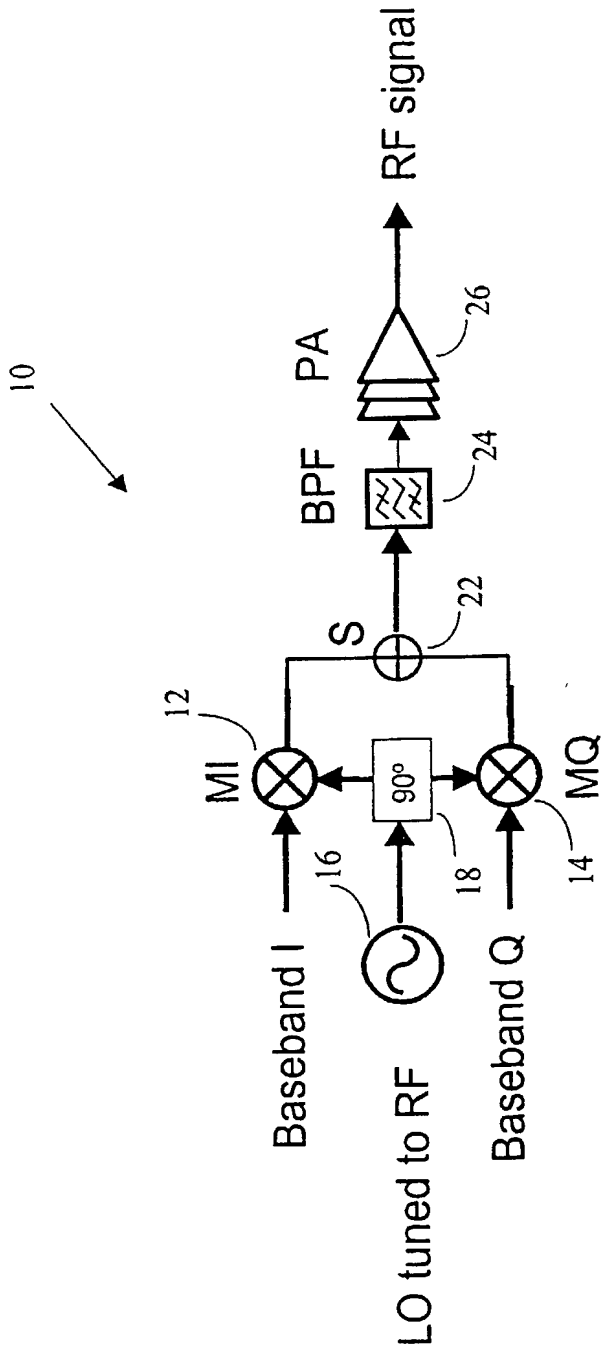

FIGURE 1 - PRIOR ART

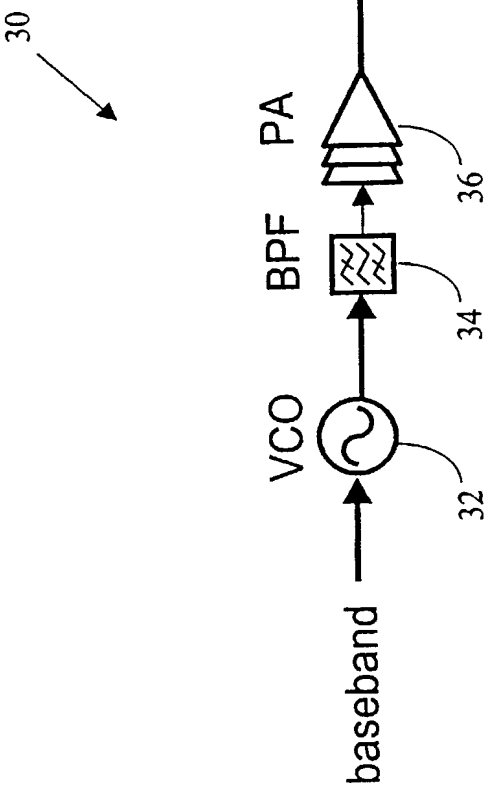

FIGURE 2 - PRIOR ART

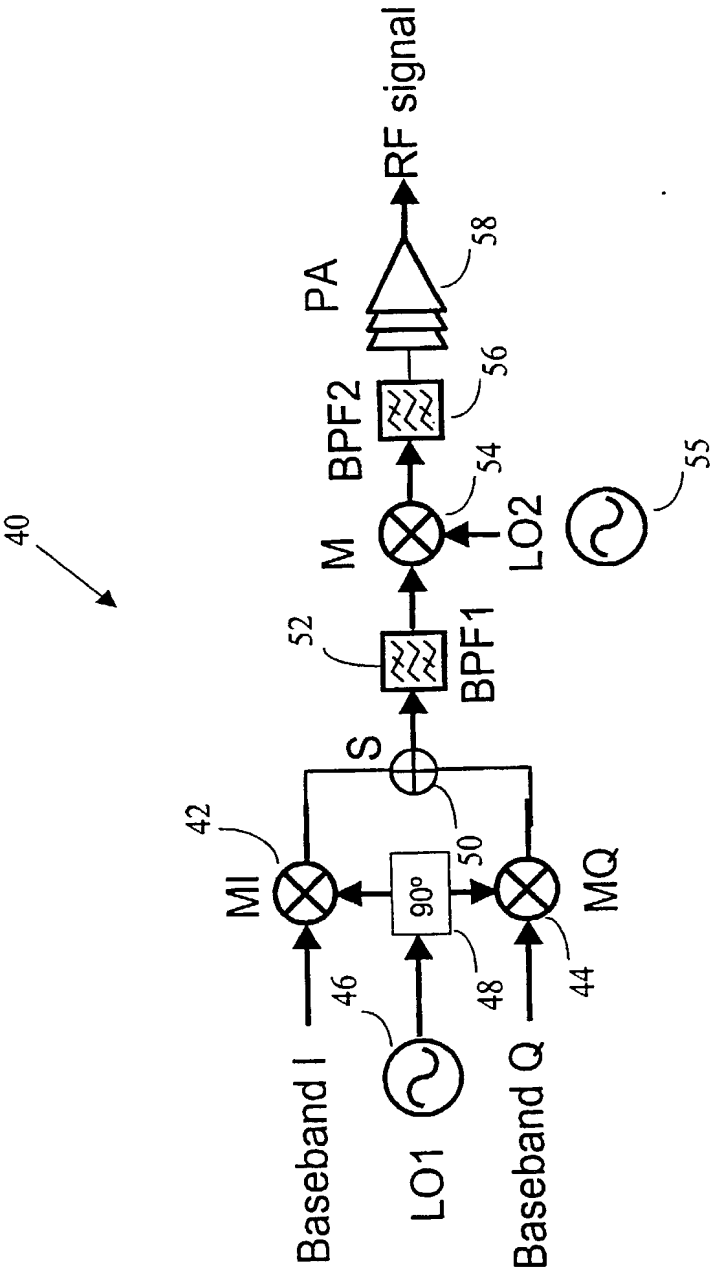

FIGURE 3 - PRIOR ART

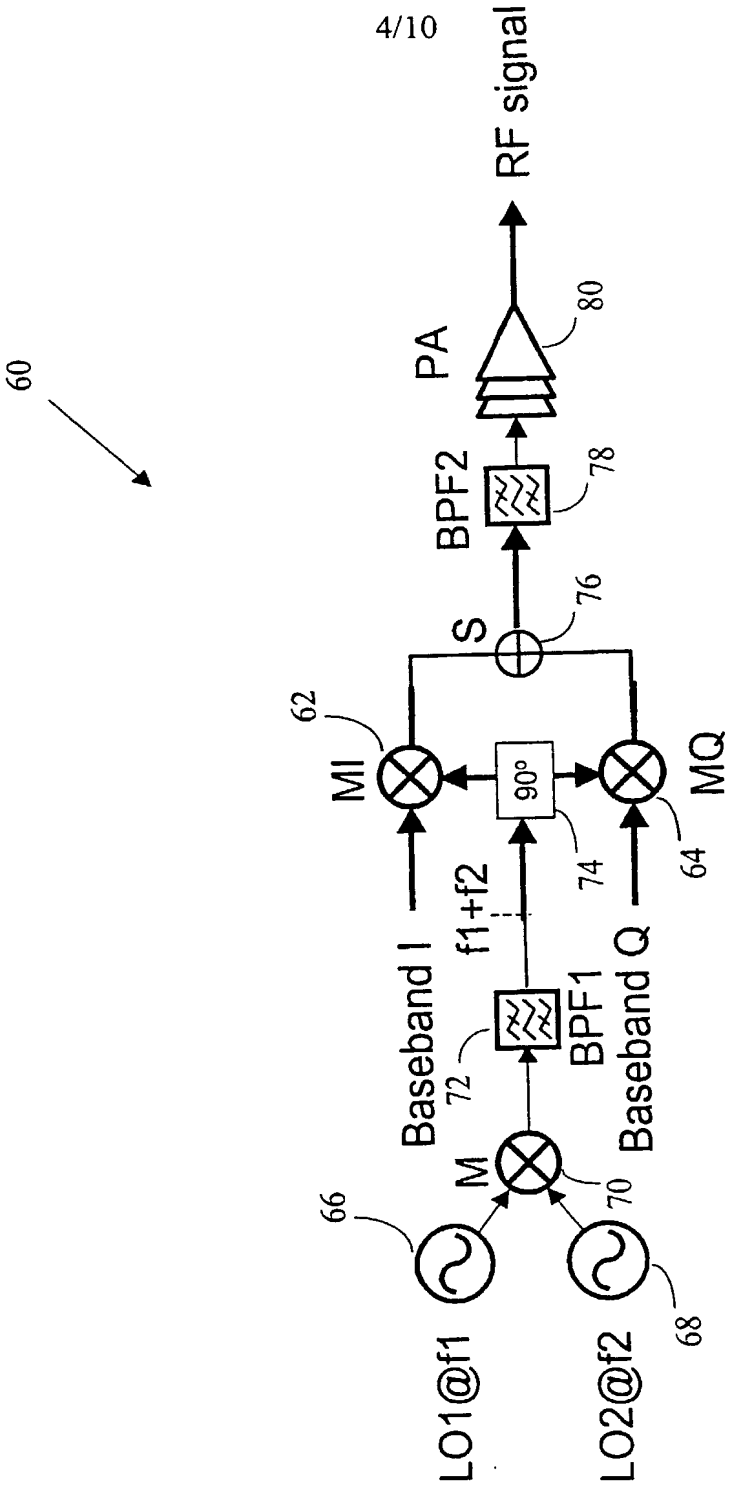

FIGURE 4 - PRIOR ART

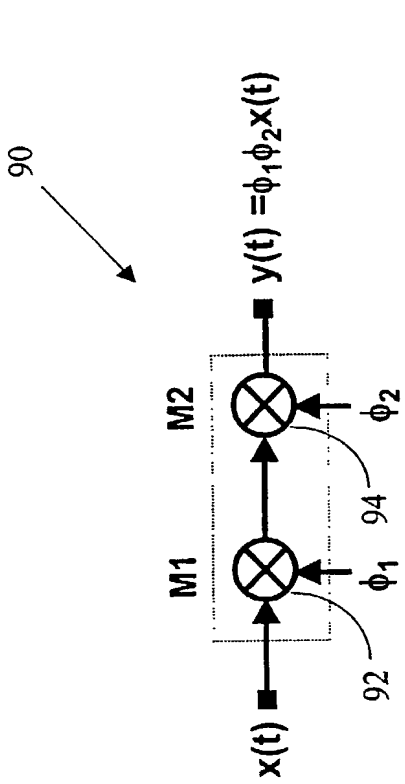

FIGURE 5(a)

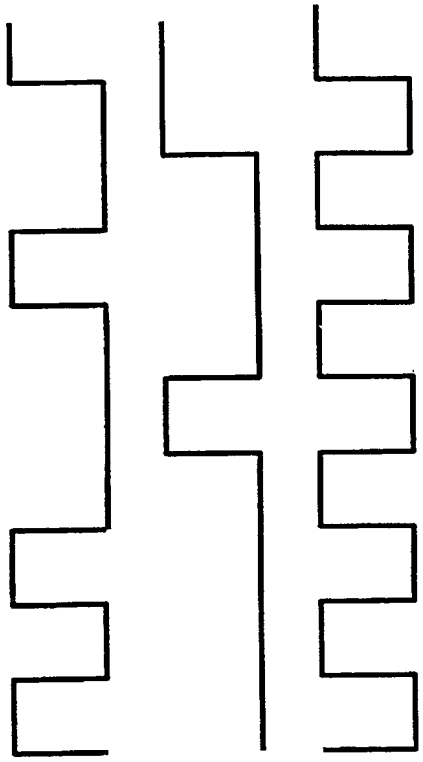

FIGURE 5(b)

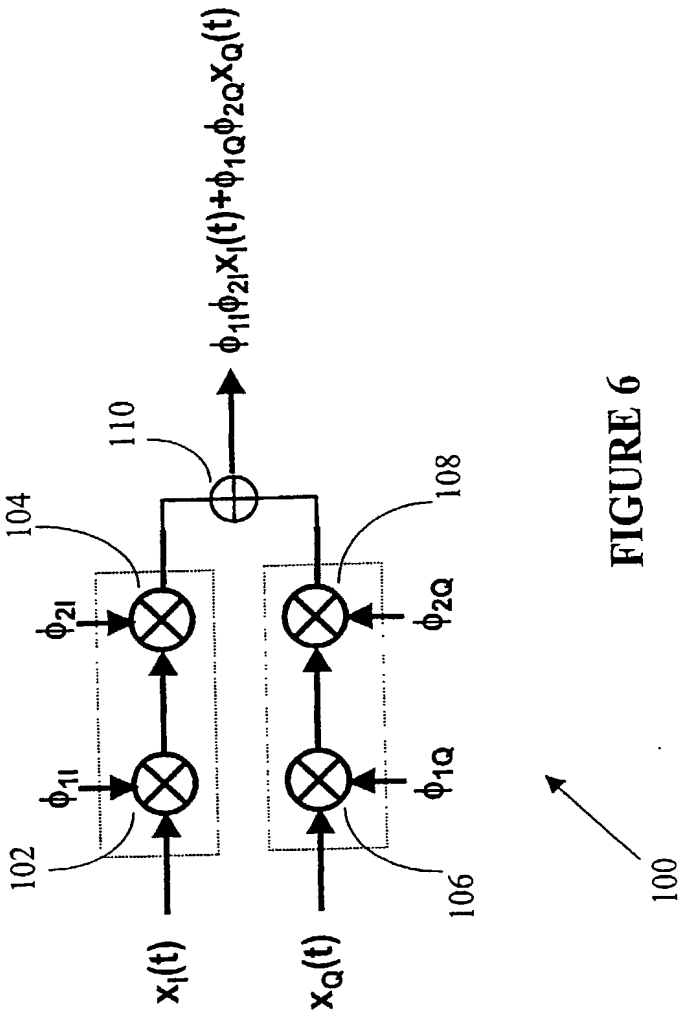
$\phi_{11}\phi_{2I}x_I(t)+\phi_{1Q}\phi_{2Q}x_Q(t)$
110
104
108
ϕ_{2I}
ϕ_{2Q}
ϕ_{1I}
ϕ_{1Q}
102
106
100
$x_I(t)$
$x_Q(t)$

FIGURE 6

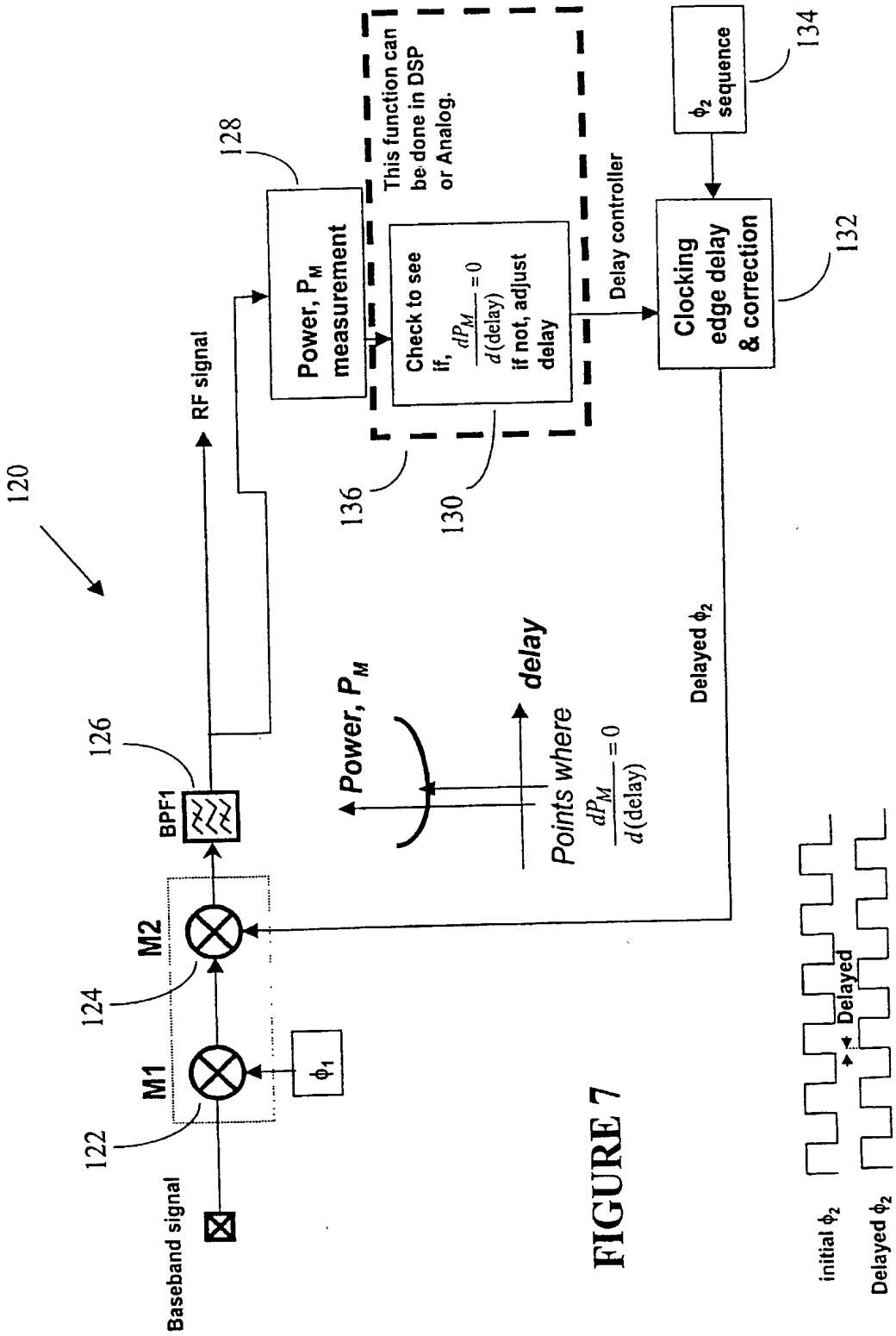
120
Baseband signal
122
M1
ϕ_1
124
M2
126
BPF1
RF signal
128
Power, P_M measurement
This function can be done in DSP or Analog.
Check to see if, $\frac{dP_M}{d(\text{delay})} = 0$ if not, adjust delay
130
136
Delay controller
ϕ_2 sequence
134
Clocking edge delay & correction
132
Delayed ϕ_2
Power, P_M
delay
Points where $\frac{dP_M}{d(\text{delay})} = 0$
Delayed
initial ϕ_2
Delayed ϕ_2

FIGURE 7

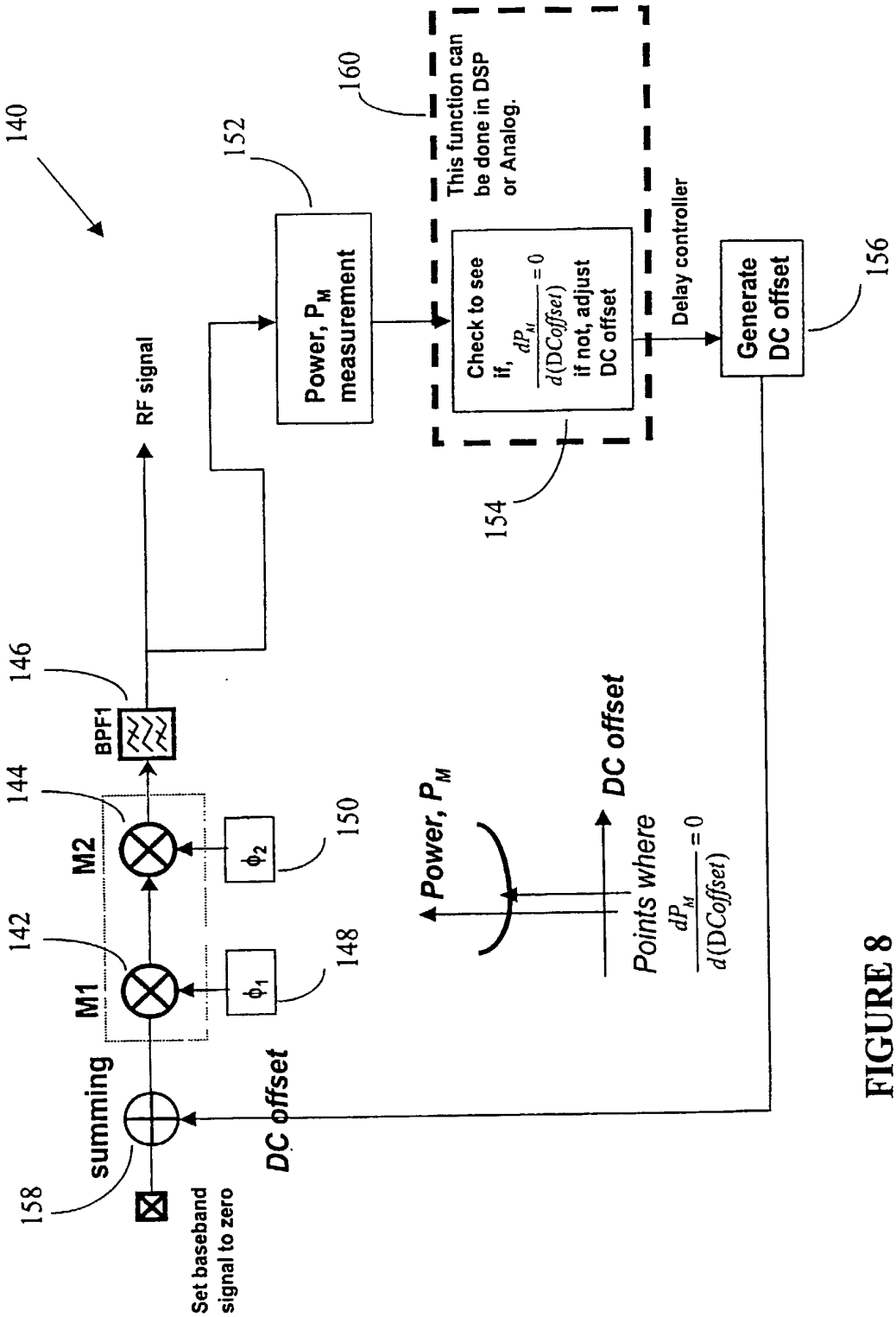
140
152
160
This function can be done in DSP or Analog.
Power, P_M measurement
Check to see if, $\frac{dP_M}{d(DCoffset)} = 0$ if not, adjust DC offset
Delay controller
Generate DC offset
156
154
RF signal
146
BPF1
144
M2
150
ϕ_2
142
M1
148
ϕ_1
summing
158
Set baseband signal to zero
DC offset
Power, P_M
DC offset
Points where $\frac{dP_M}{d(DCoffset)} = 0$

FIGURE 8

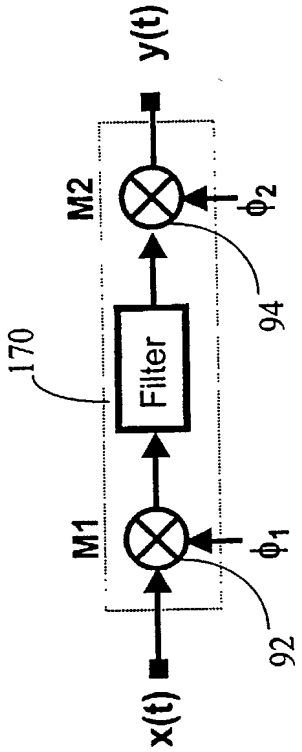

FIGURE 9

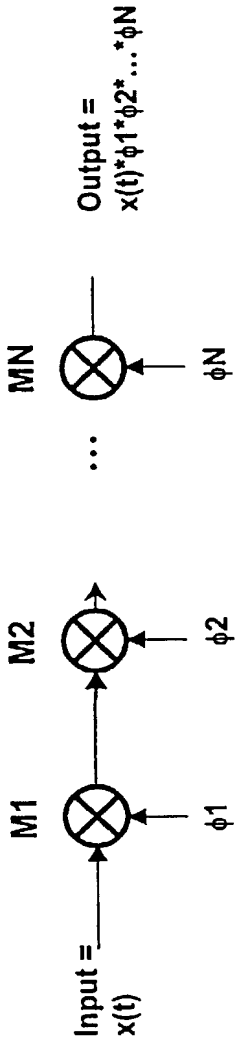

FIGURE 10

Attorney Docket No. 085907-000000US

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **IMPROVED METHOD AND APPARATUS FOR UP-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS** the specification of which ____is attached hereto or_X_was filed as **U.S. Application No. 10/070,013, the National Phase of PCT/CA00/00995, filed September 1, 2000** and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
CANADA	**2,281,236**	**September 1, 1999**	**Yes**

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

The registered attorneys and agents associated with PTO Customer No. 20350

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Tajinder Manku	Chris Snyder	Gareth Weale
Date: June 26/2002	Date: June 26, 2002	Date: 26 June 2002

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